REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicant adds new claims 11-20. Accordingly, claims 1-20 are pending in the application.

Applicant thanks the Examiner for acknowledging the claim for priority and receipt of certified copies of all the priority documents.

The Examiner is respectfully requested to state whether the drawings are acceptable.

New claims 12-20 are added to at least partially restore the original range of claims that existed before multiple dependencies were removed in the preliminary amendment. No new matter is added.

Applicant acknowledges the indication that claims 2 and 4-8 define patentable subject matter and would be allowable if rewritten in independent form, including all limitations of their base claim, and any respective intervening claims.

Reexamination and reconsideration are respectfully requested in view of the following remarks.

35 U.S.C. § 103

The Office Action rejects claims 1, 3, 9 and 10 under 35 U.S.C. § 103 over Fournel et al. U.S. Patent 5,943,264 ("Fournel") in view of Tsukamoto U.S. Patent 5,943,264 ("Tsukamoto").

Applicant respectfully traverses these rejections for at least the following reasons.

Among other things, the one-time programmable memory device of claim 1 includes ***an MOS memory transistor*** connected in series between a voltage supply line and ground, and further comprising ***programming means for applying voltages to*** a gate of a selection transistor, to ***a gate of a memory transistor*** and to a voltage supply line, ***which applied voltages force the memory transistor into a snap-back mode*** resulting in a current thermally damaging a drain junction of the memory transistor.

Applicant respectfully submits that no possible combination of Fournel and Tsukamoto could ever produce a one-time programmable memory device including these features.

At the outset, the Office Action states that Fournel discloses "*applied voltages force said memory transistor into a snap back mode resulting in a current thermally damaging a drain of said memory transistor*," citing generally the Abstract and the Summary of Invention.

Applicant respectfully submits that Fournel discloses no such thing. Instead, Fournel discloses that "*the **selection transistor** is biased in the snap-back mode*" (e.g., Abstract at lines 13-14; col. 3, lines 21-42). Fournel never discloses that ***a memory transistor*** itself is forced into a snap back mode. Indeed, as will be explained in more detail below, Fournel never even discloses a memory transistor!

Tsukamoto certainly does not disclose that any memory transistor is forced into a snap-back mode, or that Fournel should be modified to include any memory transistor is forced into a snap-back mode.

Therefore, it is not possible for any combination of Fournel and Tsukamoto to produce the one-time programmable memory device of claim 1.

Furthermore, the Office Action fairly admits that Fournel does not disclose the MOS memory transistor, but rather discloses merely a PN junction. However, the Office Action states that Tsukamoto "*shows that it is well known that a MOS transistor connected diode is functionally equivalent to a pn diode.*"

Applicant notes that, indeed, Tsukamoto teaches that in the context of its circuit, a MOS transistor whose ***gate and drain are connected together*** functions as a diode.

Accordingly, at most, a combination of Fournel and Tsukamoto would produce a one-time programmable memory device including a MOS selection transistor and a MOS memory transistor connected as a diode (i.e., with its gate and drain connected together) connected in series between a voltage supply line and ground.

However, such an arrangement cannot possibly include remaining features of claim 1.

For example, claim 1 recites programming means for applying voltages to a gate of said selection transistor, ***to a gate of said memory transistor*** and to said voltage supply line, ***which applied voltages force said memory transistor into a snap-back mode***." Clearly, no such voltage can be applied to a MOS memory transistor connected as a diode where the gate is connected to the drain!

Accordingly, for at least these reasons, Applicant respectfully submits that claim 1 is very clearly patentable over any possible combination of Fournel and Tsukamoto.

Claims 3 and 9

Claim 3 depends from claim 1 and therefore is deemed patentable for at least the reasons set forth above with respect to claim 1. Claim 9 recites CMOS circuitry including the one-time programmable memory device of claim 1, and therefore is deemed patentable for at least the reasons set forth above with respect to claim 1.

Claim 10

Among other things, the method of claim 10 includes applying voltages to a gate of a selection transistor, to a gate of a memory transistor and to a voltage supply line, which applied voltages ***force the memory transistor into a snap-back mode*** resulting in a current thermally damaging a drain junction of the memory transistor.

For similar reasons to those set forth above with respect to claim 1, no possible combination of Fournel and Tsukamoto could ever produce a method including these features.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 10 is very clearly patentable over any possible combination of Fournel and Tsukamoto.

CLAIMS 11-20

Claims 11 through 20 depend variously from claims 1 and 10 and are deemed patentable for at least the reasons set forth above with respect to claims 1 and 10. It is also noted that claim 11 recites features similar to those in claim 2, which has

already been stated to define patentable subject matter. Applicant also notes that claims 12-20 depend variously from claim 2, which has already been stated to define patentable subject matter.

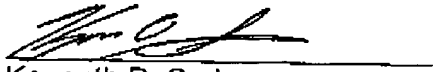
CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-20 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment (except for the issue fee) to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

VOLENTINE & WHITT

By: 
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